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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/699,222	10/31/2003	Ted Johansson	5497-105	2778

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EXAMINER	
TSAI, H JEY	
ART UNIT	PAPER NUMBER
2895	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/699,222	JOHANSSON ET AL.	
	Examiner	Art Unit	
	H.Jey Tsai	2895	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 September 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1, 3-55* is/are pending in the application.

4a) Of the above claim(s) *36-55* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/17/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3-9, 20-23, 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ammo et al. 2002/0033509, previously cited, in view of Gris 6,156,594, or Pruijimboom et al. 2002/0030244, newly cited.

The references teaches:

Ammo et al. discloses a method in the fabrication of an integrated circuit including at least one bipolar transistor and at least one MOS device comprising the steps of:

providing a silicon substrate 1, fig. 3A, para. 31-35,

forming an active region 2 for the bipolar transistor and an active region 6 for the MOS device in said silicon substrate 1, figs. 3A-3C,

forming field isolation areas 5 around, in a horizontal plane, said active regions, fig. 3A-3C,

forming a MOS gate region on said active region for the MOS device;

forming a layer of an electrically insulating nitride material 17 on said MOS gate region 7 and on said active region 2 for the bipolar transistor, para. 36-43, also see col.

4, lines 8-12, fig. 5, nitride layer 20 formed over MOS region and bipolar transistor active region,

defining a base region 18 in said active region for the bipolar transistor by means of producing an opening in said electrically insulating layer 15, wherein said opening in said electrically insulating layer 17 is produced so that the remaining portions of the electrically insulating layer partly cover said active region for the bipolar transistor, fig. 4B, para. 43-45,

electrically insulating layer 15/17 remains on said MOS gate region to encapsulate and protect the MOS gate region during subsequent manufacturing steps.

wherein said electrically insulating layer 17 is a nitride layer, para. 42.

Regarding claim 3. The method as claimed in claim 1 further comprising the step of manufacturing of a capacitor 20, wherein a portion of said electrically insulating layer is utilized as the dielectric in said capacitor.

Regarding claim 4. The method as claimed in claim 1 wherein said MOS gate region is formed as a silicon layer 13 on top of an oxide layer 12, para. 37, 38.

Regarding claim 5. The method as claimed in claim 4 wherein an oxide 15 is formed on top of the silicon layer prior to forming said electrically insulating layer 17.

Regarding claim 6. The method as claimed in claim 4 further comprising the step of forming an oxide layer 15 on top of said active region 2 for the bipolar transistor prior to forming said electrically insulating layer 17, fig. 4A.

Regarding claim 7. The method as claimed in claim 6 further comprising the step of producing said opening also through said oxide layer 15 on top of said active region so as to expose a portion of said active region for the bipolar transistor, fig. 4B.

Regarding claim 8. The method as claimed in claim 6 wherein said oxide layer 15, on top of which said gate polysilicon layer 13 is formed, and said oxide layer 15 formed on top of said active region for the bipolar transistor are formed simultaneously, fig. 3C.

Regarding claim 9. The method as claimed in claim 1 wherein said active region 11 for the MOS device is ion implanted prior to the formation of said MOS gate region, para. 36.

Regarding claim 20. The method as claimed in claim 1 wherein the bipolar transistor is an NPN-transistor and the MOS device is a PMOS transistor, para.31.

Regarding 21. The method as claimed in claim 1 further comprising the steps of: forming a buried collector region for the bipolar transistor in said substrate, said buried collector region 3 being located underneath said active region for the bipolar transistor; producing the field isolation area 5 formed around the active region for the bipolar transistor as a shallow trench (recess) in said silicon substrate, said shallow trench (etch an recess) extending vertically from the substrate surface and down into the buried collector region; and filling said shallow trench with an electrically insulating material 5, para. 34.

Regarding claim 22. The method as claimed in claim 21 wherein said buried collector region 3 and said shallow trench5 are formed relative each other so that said

buried collector region 3 extends into areas located underneath said shallow trench 5, figs. 3A-3B.

Regarding claim 23. The method as claimed in claim 22 wherein said buried collector region is strongly n-doped (N+), para. 32.

Regarding claim 29. The method as claimed in claim 1 wherein said subsequent manufacturing steps include a step of oxidation, ion implantation, or etching, para. 40, 45, 47.

Regarding claim 30. The method as claimed in claim 8 wherein said oxide layer, on top of which said gate polysilicon layer is formed (para. 40, fig. 3C), and said oxide layer 12 on top of said active region for the bipolar transistor are grown, para. 37, fig. 3B 15.

The difference between the references applied above and the instant claim(s) is: Ammo et al. teaches forming a nitride layer over MOS gate region and active region but does not teach the remaining of nitride layer partly cover the active region of bipolar transistor. However, Gris teaches at col. 4, lines 8-12 and fig. 5, remaining of nitride layer 20 partly cover the active region of bipolar transistor after forming opening. Pruijimboom et al. teaches at para. 23, remaining of nitride layer 15 partly cover the active region of bipolar transistor after forming opening.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the above references' teachings by leaving the remaining of nitride layer partly cover the active region of bipolar transistor after forming base

opening as taught by Gris or Pruijimboom et al. because nitride layer protect the MOS and bipolar device.

Claims 10-19 are rejected under 35 U.S.C 103 as being unpatentable over Ammo et al. in view of Gris or Pruijimboom et al. as applied to claims 1-9, 21-23, 29-30 above, and further in view of Hutter et al. 6,432,791.

The difference between the references applied above and the instant claim(s) is: Ammo et al. teaches a secondary implanted collector 8 in said active region 2 for the bipolar transistor and a background doping 9 of said active region for the capacitor 7 are formed simultaneously in an ion implantation step, (claim 10), an extrinsic base 19 for the bipolar transistor is formed on said electrically insulating layer and partly on said active region for the bipolar transistor in said opening to thereby define an emitter opening, said extrinsic base being formed prior to said ion implantation step and being protected by oxide layer during said ion implantation step, para. 43-45, (claim 11), extrinsic base is doped and source and drain regions are formed in said active region for the MOS device simultaneously in an ion implantation step (claim 12), an electrode 20 of a capacitor or a contact layer for a substrate contact is doped in the ion implantation step, in which said extrinsic base 19 is doped, para. 43, (claim 13), a silicon oxide 15 and silicon nitride 17 bi-layer is formed on said doped source and drain regions to thereby prevent implanted species from diffusing out of said active region, fig. 4B, (claim 14) but does not teach simultaneously implanting collector and background of MOS device, using photoresist to protect extrinsic base during emitter implantation,

simultaneously implanting extrinsic base and source/drain regions. However, Hutter teaches at 2q, col. 2, lines 18-32, simultaneously implanting collector 202 and background 202 of MOS device (meeting claim 10). Hutter teaches at fig. 2p, col. 4, lines 38-67, using photoresist 244 or 252 to protect extrinsic base 250 (meeting claim 11), simultaneously implanting extrinsic base and source/drain regions (meeting claim 12). Hutter teaches at fig. 2b, 2n, col. 4, lines 42-46, implanting different dopant arsenic and phosphorous to form deep collector plug 208 and active region with energy and dose (meeting claims 15, 16, 17, 18. Hutter teaches at col. 4, lines 50-67, implanting to form a resistor.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the above references' teachings by simultaneously implanting collector and background of MOS device, using photoresist to protect the extrinsic base and simultaneously implanting extrinsic base and source/drain regions, implanting different dopant to form collector plug and a resistor as taught by Hunter et al. because simultaneously implanting different regions would reduce the process steps, using photoresist over extrinsic base would protect extrinsic base from emitter dopants, implanting different dopant to form collector plug so that a deep plug can be obtain and a resistor can be formed with the same implanting step.

Claims 24, 27, 28 and 35 are rejected under 35 U.S.C 103 as being unpatentable over Ammo et al. in view of Gris or Pruijimboom et al. as applied to claims 1-9, 20-23, 29-30 above, and further in view of Asai et al. 6,455,364.

The difference between the references applied above and the instant claim(s) is: Ammo et al. teaches forming an isolation region but does not teach forming a deep isolation trench in shallow trench isolation, a retrograde collector region and intended use for radio frequency. However, Asai et al. teaches at fig. 1 and col. 11, lines 49-67, forming a deep trench isolation 105/106 in the shallow trench isolation 103 and a retrograde collector region 101. And, Asai et al. also teach intended use of integrated BiCMOS device for high frequency telecommunication (radio).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the above references' teachings by a deep trench isolation trench and a retrograde collector region, using integrated circuit device for radio frequency (telecommunication) as taught by Asai et al. because deep trench isolation region would completely isolate each transistor so that preventing any current leakage between each transistor, and, retrograded collector region would reduce large current spike in the collector region.

Claims 25-26 are rejected under 35 U.S.C 103 as being unpatentable over Ammo et al. in view of Gris or Pruijimboom et al. as applied to claims 1-9, 20-23, 29-30 above, and further in view of Capilla 6,137,154.

The difference between the references applied above and the instant claim(s) is: Ammo et al. teaches doping base region, buried region, an active region and collector of bipolar transistor but does not teach doping the base and collector region having fully depleted with a specific base-collector voltage. However, Capilla teaches at col. 5, lines 22-35, biasing the base and collector region at greater than 0.5 to deplete the bias-collector region.

And, specific biased voltage and doping concentration as claimed are taken to be obvious since these are variables of art recognized importance which are subject to routine experimentation and optimization and discovery of an optimum value for a known process is obvious. In re Aller, 105 USPQ 233 (CCPA 1955). And, even if applicants' modification results in great improvement and utility over the prior art, it may still not be patentable if the modification was within the capabilities of one skilled in the art, In Re Sola 25 USPQ 433.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the above references' teachings by having a specific doping concentration and bias voltage to base and collector regions as taught by Capilla because biasing base to collector region with specific voltage would fully deplete the base to collector region so that the gain of the transistor is increased.

Claims 31-34 are rejected under 35 U.S.C 103 as being unpatentable over Ammo et al. in view of Gris or Pruijimboom et al. as applied to claims 1-9, 20-23, 29-30 above, and further in view of Ohnishi et al. 6,399,993.

The difference between the references applied above and the instant claim(s) is: Ammo et al. teaches doping buried region, an active region and collector of bipolar transistor but does not teach specific doping concentration. However, Ohnishi et al. teaches at col. 7, lines 43-57, buried region 4 doping concentration at greater than 1 x 10^{19} cm^3 and doping concentration for active region/collector 9 at greater than 1E17 cm^3.

And, specific doping concentration as claimed are taken to be obvious since these are variables of art recognized importance which are subject to routine experimentation and optimization and discovery of an optimum value for a known

process is obvious. In re Aller, 105 USPQ 233 (CCPA 1955). And, even if applicants' modification results in great improvement and utility over the prior art, it may still not be patentable if the modification was within the capabilities of one skilled in the art, In Re Sola 25 USPQ 433.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the above references' teachings by doping buried region at greater than 1 x 10^{19} cm^3 and doping concentration for active region/collector at greater than 1E17 cm^3 as taught by Ohnishi et al. because specific doping concentration can be optimized to obtained a desired device performance of the device.

Conclusions

Applicant's arguments filed Sept. 8, 2008 have been fully considered but they are not persuasive. *Because newly cited references Gris and Pruijimboom et al. teaches the remaining of nitride layer partly cover the active region of bipolar transistor after forming opening in the bipolar active region as set forth above.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to H. Jey Tsai whose telephone number is (571) 272-1684. The examiner can normally be reached on from 7:00 Am to 4:00 Pm., Monday thru Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew Richards, 571-272-1736.

The fax phone number for this Group is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published

applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/H. Jey Tsai/

Primary Examiner, Art Unit 2895

11/20/2008